Application No. 09/591,044
Filed: June 9, 2000
TC Art Unit: 2112
Confirmation No.: 2567

REMARKS

The instant Amendment is filed in response to the official action dated February 25, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows.

Claims 1-9 are pending in the application.

Claims 1-9 stand rejected.

Claims 1-3 and 6-8 have been amended.

Claims 4-5 and 9 have been canceled without prejudice.

The Examiner has rejected claims 1-4 and 6-9 under 35 U.S.C. 102(e) as being anticipated by Sotek *et al.* (USP 6,209,022). Specifically, regarding base claims 1 and 6, the official action indicates that the Sotek reference discloses a system for transferring data between a plurality of devices comprising a bus including a data line and a clock line, and at least one first device coupled to the bus, in which the first device is operative (1) at a first clock rate and at a second reduced clock rate, (2) to receive a portion of the data transmitted over the data line and to store the data in a register, and (3) in the event the first device is operating at the second reduced clock rate, to drive the clock line to a predetermined logic level while the data is stored in the register, thereby enabling data transfer between

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the first device and at least one second device over the bus (see also column 7, lines 1-21, and column 5, lines 18-25, of Sotek et al.).

The official action further indicates on pages 4-5 that the Sotek reference discloses that the clock generated on the clock line of the master station can be set to two different values, a lower clock rate for a first operating mode at which output circuits OC are actuated, and a higher clock rate for a second mode of operation at which data is stored in memories. The official action concludes that such disclosure reads on the language of base claims 1 and 6.

The Applicants respectfully submit, however, that the Sotek reference does not teach or suggest a system for transferring data between a plurality of devices coupled to a bus, in which a first device operating at a first clock rate transmits data over a data line of the bus, and a second device operating at a second reduced clock rate (1) receives at least a portion of the data transmitted over the data line, (2) stores the data in a data register included in the second device, and (3) drives a clock line of the bus to a predetermined logic level while the data is stored in the data register, as recited in amended claim 1. Because amended claim 6 is the method analog of amended claim 1, the Applicants

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further submit that the Sotek reference does not teach or suggest the method of amended claim 6. Such a system and method for transferring data between devices coupled to a two-line bus, such as the System Management Bus (SMBus), are described throughout the instant application, *e.g.*, see page 12, line 5, to page 15, line 6, of the application.

Although the official action indicates that the clock line of the Sotek system can be set to lower and higher clock rates for operating in first and second modes, respectively (see page 5 of the official action), the Applicants respectfully point out that such disclosure does not anticipate the subject matter of amended claims 1 and 6. For example, amended claim 1 recites that *the second device* is operative at a first clock rate and at a second reduced clock rate; amended claim 1 does not recite that the rate of the clock signal carried by the clock line is set to two different values, as indicated in the official action. Amended claim 1 further recites that the second device drives the clock line to a predetermined logic value while operating at the second reduced clock rate. Clearly, driving a clock line to a predetermined logic level is not the same as setting a clock rate to a lower value.

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Such driving of the clock line to a predetermined logic level while the data is stored in the data register is depicted in Fig. 4 of the instant application. As shown in Fig. 4, the clock line, *i.e.*, the SCL line, is driven to a low logic level from time **T7** to time **T8**. Further, as described in the application, the clock stretcher **502** included in the network interface adapter (NIA) **304** (which is disclosed as one of the plurality of devices coupled to the bus, *i.e.*, the SMBus) extends the low period of the clock signal on the SCL line **307** from **T7** to **T8** to give the device additional clock cycles during which to complete a read operation, *i.e.*, to read the registered data on the REG_DATA line (see page 14, lines 17-23, and Figs. 3-4, of the application). Accordingly, the clock signal on the SCL line is not set to a lower clock rate between the times **T7-T8**, but is instead maintained at the low logic level from **T7** to **T8** to give the NIA **304** additional time to read the registered data on the REG_DATA line, particularly, when the NIA **304** is operating at the second reduced clock rate (see page 11, lines 8-15, of the application).

The Applicants respectfully submit that their system as claimed is fundamentally different from the system disclosed in the Sotek reference. For example, as described in the instant application, the SCL line is driven to the low logic level to

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extend the low period of the clock signal, thereby enabling data transfer between devices coupled to the SMBus by giving at least one of the devices additional clock cycles to complete a data read operation (see page 14, lines 17-23, and Fig. 4, of the application). In contrast, the Sotek reference merely discloses that the clock rate on a clock line is set to two different values, namely, a lower clock rate for a first operating mode in which first output circuits OC are actuated, and a higher clock rate for a second operating period, in which data stored in data memories MEM can be transmitted via corresponding second output circuits TR (see column 6, lines 35-42, of Sotek *et al.*).

Moreover, the Applicants point out that, whereas the second device of amended claims 1 and 6 is operative at the first clock rate and at the second reduced clock rate, *e.g.*, when executing a power management application (see page 10, lines 16-28, of the application), the lower clock rate of the Sotek system has nothing to do with implementing power management functions. Instead, Sotek *et al.* employ the lower clock rate simply because a plurality of open-collector output circuits included in their system cannot handle the higher switching speed.

Because the Sotek reference does not describe a system that includes a device coupled to a bus that, in the event it is

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operating at a reduced clock rate, *drives a clock line* to a predetermined logic level while data is stored in a data register within the device, thereby enabling data transfer between the device and at least one other device coupled to the bus, the Sotek reference does not anticipate amended claims 1 and 6 and the claims dependent therefrom. Accordingly, the Applicants respectfully submit that the rejections of these claims under 35 U.S.C. 102(e) is unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of

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the present application.

Respectfully submitted,

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